DETAILED ACTION

1. Claims 1-87 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims1-87 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 1, it claims for an instruction that is able to de-schedule, de-allocate, or reschedule a thread depending on what a first parameter is. If this instruction is the same as the YIELD instruction, then according to the specification, the YIELD instruction can only take in one parameter. As disclosed in Para 111 of the applicant's published application, it states that the YIELD instruction only takes a single parameter contained in "rs". However, the claim claims for another second parameter. The specification does not describe a second parameter in the YIELD instruction.

If the “an instruction” in the claim is not the same as the YIELD instruction, then the specification does not disclose another thread that is able to de-schedule, de-allocate, or reschedule a thread.

Claims 2-87 have the same deficiencies as above.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following claim languages are unclear and indefinite:

1) Claim 1, it is uncertain if “an instruction” in line 3 and the ‘yield instruction” in the last line are the same instruction (i.e. if they are the same instruction, then the claim is unsupported by the specification as described above because the YIELD instruction, according to the specification, can only take in one parameter. If they are different instructions, then the claims still does not make any sense because according to the specification, the YIELD instruction is supposed to de-schedule, deallocate or reschedule the thread. If the "an instruction" is doing these things, then what is the YIELD instruction doing?)

Claims 2-87 have the same deficiencies.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 15, 29, 42, 56, 75, 76, 84, 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hapner et al., Patent No. 5,727,203 (hereafter Hapner) in view of Sprangle et al., Patent No., 6,925,550 (hereafter Sprangle) further in view of Sasaki et al., European Patent Publication No. 0256149B1 (hereafter Sasaki).

6. Hapner and Sprngle were cited in the previous office action.

7. As per claim 1, 15, 29, 42, 56, 75, 76, 84, 86, Hapner teaches a multi-threading processor mechanism, comprising:

A data storage device configured to store a parameter (Column 12, line 31); and

A program thread configured to deschedule itself, to deallocate itself, or to reschedule itself to resume execution, and the thread enabled to access the parameter (Column 12, lines 31-52; Column 12, lines 57-63; Column 14, lines 1-7);

Wherein, when a portion of the parameter equals a first value, the program thread to resume execution in accordance with one or more conditions encoded within the parameter (Column 12, lines 31-52).

Hapner does not specifically teach that the thread contains an instruction that is responsible for descheduling, deallocating, or rescheduling, and the instruction being able to access the parameter.

However, Sprangle teaches an instruction that is responsible for descheduling, deallocating, or rescheduling, and the instruction being able to access the parameter for the purpose of achieving conditional execution (Column 3, lines 22-30; Column 5, lines 5-23).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Hapner with the specifics of an instruction that is responsible for descheduling, deallocating, and rescheduling, and the instruction being able to access the parameter, as taught by Sprangle, because it allows for conditional execution.

Hapner in view of Sprangle does not specifically teach a second parameter configured for receiving a result value of the instruction usable by a yield instruction of the program thread.

However, Sasaki teaches a second parameter configured for receiving a result value of the instruction usable by a yield instruction of the program thread for the purpose of stopping a thread for a specified amount of time (Column 4, lines 31-50: the pause instruction corresponds to the yield instruction).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Hapner in view of Sprangle with the specifics of a second parameter configured for receiving a result value of the instruction usable by a yield instruction of the program thread, as taught by Sasaki, because it allows for the system to stop a thread for a specified amount of time.

8. Claims 1, 15, 29, 42, 56, 75, 76, 84, 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer et al., U.S. 6,675,129 (hereafter Emer) in view of Shimada, U.S. 6,687,812 (hereafter Shimada) further in view of Sasaki et al., European Patent Publication No. 0256149B1 (hereafter Sasaki).

9. Emer and Shimada were cited in the previous office action.

10. As per claim 1, 15, 29, 42, 56, 75, 76, 84, 86, Emer teaches a multi-threading processor mechanism, comprising:

A data storage device configured to store a parameter (Column 8, lines 35-47);

An instruction disposed within a program thread, the instruction configured to suspend the program thread and the instruction enabled to access the parameter (Column 5, lines 41-47; Column 8, lines 35-47).

Emer does not specifically teach that the instruction may also be configured to de-schedule the program thread, to deallocate the program thread and to reschedule the program thread to resume execution and wherein, when the parameter equals a first value the instruction reschedules the program thread to resume execution in accordance with one or more conditions encoded within the parameter.

However, Shimada teaches that the instruction may also be configured to de-schedule the program thread, to deallocate the program thread and to reschedule the program thread to resume execution and wherein, when the parameter equals a first value the instruction reschedules the program thread to resume execution in accordance with one or more conditions encoded within the parameter for the purpose of allowing further options for the thread as to what it should do under various circumstances (Column 3, lines 34-45; Column 14, lines 6-16, lines 22-30, 44-51).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Emer with the additional capability of that the instruction may also be configured to de-schedule the program thread, to deallocate the program thread and to reschedule the program thread to resume execution and wherein, when the parameter equals a first value the instruction reschedules the program thread to resume execution in accordance with one or more conditions encoded within the parameter, as taught by Shimada, because this allow further options for the thread as to what it should do under various circumstances.

Shimada in view of Emer does not specifically teach a second parameter configured for receiving a result value of the instruction usable by a yield instruction of the program thread.

However, Sasaki teaches a second parameter configured for receiving a result value of the instruction usable by a yield instruction of the program thread for the purpose of stopping a thread for a specified amount of time (Column 4, lines 31-50: the pause instruction corresponds to the yield instruction).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Shimada in view of Emer with the specifics of a second parameter configured for receiving a result value of the instruction usable by a yield instruction of the program thread, as taught by Sasaki, because it allows for the system to stop a thread for a specified amount of time.

11. Claims 2-14, 16-28, 30-41, 43-55, 57-64, 65-74, 77-83, 85, 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hapner et al., Patent No. 5,727,203 (hereafter Hapner) in view of Sprangle et al., Patent No., 6,925,550 (hereafter Sprangle) further in view of Sasaki et al., European Patent Publication No. 0256149B1 (hereafter Sasaki) further in view of Dupree et al (Dupree), Patent No. 5,949,994.

12. Dupree was cited in the previous office action.

13. As per claims 16, 2, 30, 43, 57, Hapner in view of Sprangle further in view of Sasaki does not specifically teach wherein the data storage device is a general purpose register (GPR).

However, Dupree teaches wherein the record is in a general purpose register (GPR) for the purpose of storing the status message. *(Column 30, lines 60- Column 31 lines 60; Moreover a GPR is a data storage)*

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Hapner in view of Sprangle further in view of Sasaki with the specifics of wherein the record is in a general purpose register (GPR), as taught by Dupree, because it allows for the storage of status messages.

14. As per claims 17, 3, 31, 44, 58, 87, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being deallocated rather than rescheduled. *(Column 27, lines 45-52)*

15. As per claims 18, 4, 32, 45, 59, 77, Dupree teaches the method of claim 17 wherein the parameter associated with the thread being deallocated is a value of zero. *(Fig 4B: no NAND gates. Column 25, lines 10-16: setting a bit and the fact that there is no NAND gate in the circuit means asserted high for scheduling. Therefore, zero for deallocation.)*

16. As per claims 19, 5, 33, 46, 60, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being requeued for scheduling. *(Column 32, lines 40-61; Column 25, lines 10-16)*

17. As per claims 20, 6, 34, 47, 61, Dupree teaches the method of claim 19 wherein the parameter is any-odd-value. *(Column 25, lines 10-16: the thread to be scheduled must have its scheduling bit set to 1, which is an odd value.)*

18. As per claims 22, 49, 63, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread relinquishing execution to another thread until a specific condition is met *(Column 26, lines 15-30)*

19. As per claims 23, 9, 50, 64, Dupree teaches the method of claim 22 wherein the parameter is encoded in one of a bit vector or one or more value fields in the record. *(Column 25, lines 10-16, Column 31, lines 5-60)*

20. As per claims 24, 10, 51, Dupree teaches wherein the processing further comprises resuming execution of the one of the plurality threads. *(Column 27, lines 45-67, Column 32, lines 20-60)*

21. As per claim 25, 38, 52, 65, Dupree teaches the method of claim 15 wherein one or more of the parameters is associated with one of the plurality of threads being deallocated rather than rescheduled, and another of the parameters is associated with the thread being requeued for scheduling. *(Column 27, lines 45- 67: the PC is set for interrupt if to be rescheduled, which corresponds to another parameter. The a bit for the thread in the scheduler latch would be unset if the thread is to be deallocated.)*

22. As per claim 26, 8, 39, 53, 66, Dupree teaches the method of claim 15 wherein one or more the parameters is associated with one of the plurality of threads being deallocated rather than rescheduled, and another of the parameters is associated with relinquishing execution to another thread until a specific condition is met. *(Column 27, lines 45- 67: relinquish until condition is met corresponds to rescheduling.)*

23. As per claim 27, 40, 54, 67, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being requeued for rescheduling, and another of the parameters is associated with relinquishing execution to another thread until a specific condition is met. *(Column 27, lines 45- 67: The two scenarios are equivalent since after the condition is met, the thread must be rescheduled.)*

24. As per claim 28, 41, 55, 68, Dupree teaches the method of claim 15 wherein one of the parameters is associated with the thread being deallocated rather than rescheduled, another of the parameters is associated with the thread being requeued for scheduling, and another of the parameters is associated with relinquishing execution to another thread until a specific condition is met. *(Column 27, lines 45- 67: The two scenarios are equivalent since after the condition is met, the thread must be rescheduled.)*

25. As per claim 11, Dupree teaches the mechanism of claim 3 wherein, when the parameter equals a third value, the third value being different from the first and second values, the instruction unconditionally reschedules the program thread. *(Column 23, lines 1- 5, Column 25, lines 50- 67, Column 26, lines 15-30: there are different states for a context. When it is in the bidding state, the context has been scheduled unconditionally, and has an interrupt pending. Each state is represented by different values.)*

26. As per claim 12, Dupree teaches the mechanism of claim 1 wherein one of the one or more conditions is a hardware interrupt. *(Column 25, lines 9-30)*

27. As per claim 13, Dupree teaches the mechanism of claim 1 wherein one of the one or more conditions is a software interrupt. *(Column 25, lines 50-57)*

28. As per claim 14, Dupree teaches the mechanism of claim 1 wherein, in the circumstance of the program thread being rescheduled, execution of the program thread resumes at a place in the thread following the instruction. *(Column 27, lines 45-67, Column 32, lines 20-60)*

29. As per claim 36, Dupree teaches the digital processor of claim 29 wherein one of the parameters is associated with the thread relinquishing execution to another thread until a specific condition is met. *(Column 25, lines10-17, lines 50- 67; Column 26, lines 3- 15; Column 27, lines 45-67: relinquishing until a condition is met corresponds to interrupt and its service routines followed by rescheduling.)*

30. As per claim 37, Dupree teaches the digital processor of claim 36 wherein the parameter is encoded in one of a bit vector or one or more value fields in the record. *(Column 25, lines 10-20, Column 27, lines 45-67: latch and registers all corresponds to bit vector.)*

31. As per claim 69, 72, 73, 74, Dupree teaches the mechanism of claim 1 wherein the instruction is a YIELD instruction. *(Column 27, lines 55-65: The inherent instruction issued to access the status of scheduler latch corresponds to the YIELD instruction.)*

32. As per claim 70, Dupree teaches the mechanism of claim 1 wherein the portion of the record comprises a bit vector. *(Column 25, lines 10-20, Column 27, lines 45-67: latch and registers all corresponds to bit vector.)*

33. As per claim 71, Dupree teaches the mechanism of claim 1 wherein the portion of the record comprises one or more multi-bit fields. *(Column 25, lines 10-20, Column 27, lines 45-67)*

34. As per claim 78, Dupree teaches the method of claim 76 further comprising suspending the program thread from execution in response to the instruction when the parameter equals a second value, wherein the second value is different from the first value. *(Column 23, lines 1-5, Column 25, lines 50- 67, Column 26, lines 15- 30: there are different states for a context. The bidding state corresponds to thread suspension. When it is in the bidding state, the context has been scheduled unconditionally, and has an interrupt pending. Each state is represented by different values.)*

35. As per claim 79, Dupree teaches the method of claim 78 wherein the second value indicates that a condition required for execution of the program thread is

unsatisfied. *(Column 23, lines 1-5, Column 25, lines 50- 67, Column 26, lines 15-30: So long as an interrupt is pending, it is an indication that requirements for execution is unsatisfied.)*

36. As per claim 80, Dupree teaches the method of claim 79 wherein the condition is encoded within the parameter as a bit vector or value field. *(Column 25, lines 10-20, Column 27, lines 45-67: latch and registers all corresponds to bit vector.)*

37. As per claim 81, Dupree teaches the method of claim 78 further comprising rescheduling the program thread in response to the instruction when the parameter equals a third value, wherein the third value is different from the first and second values. *(Column 23, lines 1- 5, Column 25, lines 50-67, Column 26, lines 15-30: The idle state and its information corresponds to the third value.)*

38. As per claim 83, Dupree teaches the method of claim 81 wherein the third value is an odd value. *(Column 25, lines 10-16: the thread to be scheduled must have its scheduling bit set to 1, which is an odd value.)*

39. As per claim 85, Dupree teaches the method of claim 84 further comprising rescheduling the program thread in response to the instruction when the parameter equals a second value, wherein the second value is different from the first value. *(Column 25, lines 10- 20: bit is set to one for rescheduling.)*

40. As per claim 21, 7, 35, 48, 62, 82, Dupree teaches all of claim 19. Moreover, he teaches using two different numbers, 1 and 0, to represent the presence of a scheduled event and no event is being scheduled, respectively *(Column 25, lines 10- 15; Column 27, lines 45-67)*. However, he does not specifically state that wherein the parameter is a two's compliment value of negative 1. It is well known that using two's compliment is a mere way of representing a number. Furthermore, any number can be used in a register to indicate an event. It does not matter if it is negative 1 or 1, as long as it is different from another number used to indicate a different type of event. The applicant fails to demonstrate any unexpected results from the use of negative one that cannot also be achieved with the differing values taught by Dupree.

Response to Arguments

41. Applicant's arguments with respect to claims 1-87 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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